Product Brief

Marvell® Prestera® 98DX85xx Multi-Layer Ethernet Switches

A new generation of highly-integrated packet processors for Enterprise LAN access and aggregation

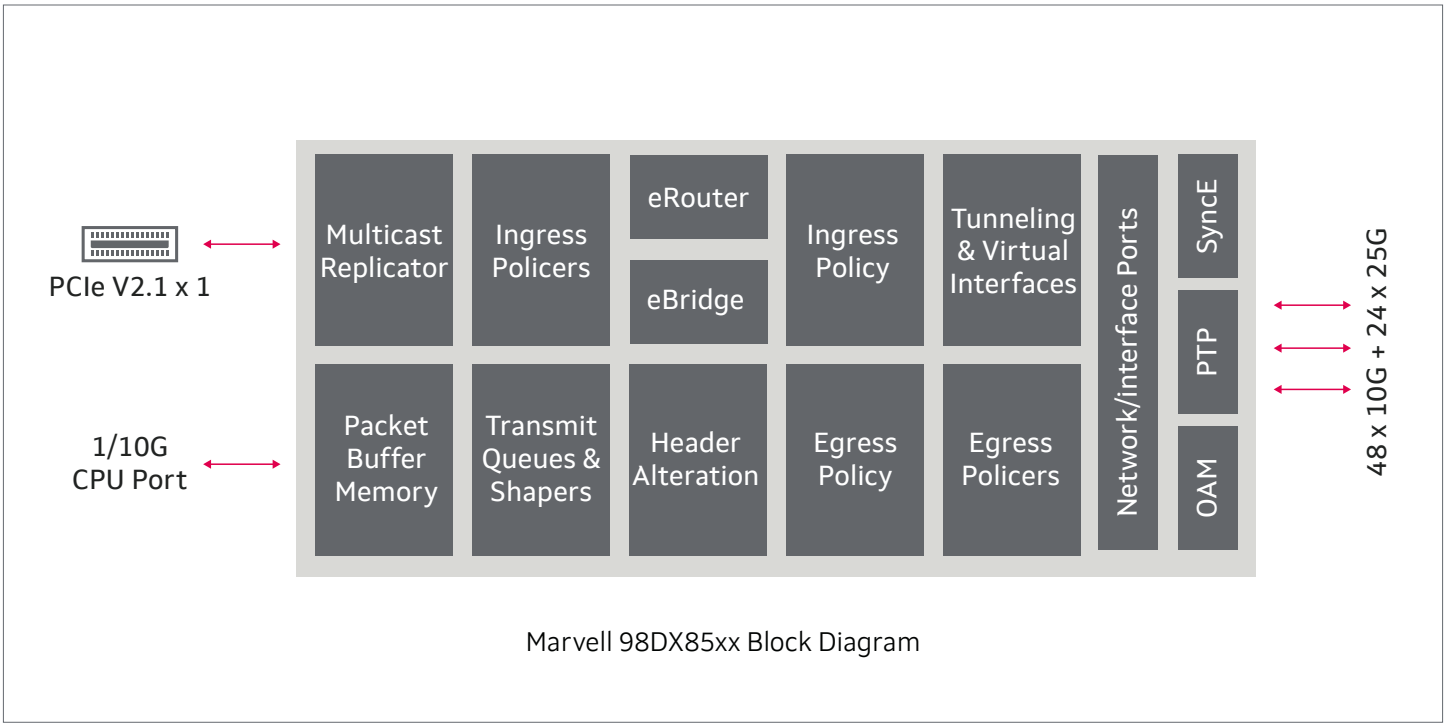
Overview

The Prestera® 98DX85xx multi-layer Ethernet switch family is a new generation of highly-integrated packet processors. They are built for service delivery in various applications, such as: Campus LAN Access and Aggregation Switch, Wi-Fi 802.11ac Wave2 Access Point Aggregation, eDrive and Server connectivity, and other interconnect applications requiring low-power 100 GbE, 40 GbE, 25 GbE, and 10 GbE embedded connectivity.

The 98DX85xx supports advanced packet processing features, such as virtual overlay networking with programmable tunnel header encapsulation, NFV service function chaining, low latency cutthrough switching, dynamic load balancing, and advanced congestion mechanisms. Its architecture enables the key technologies, such as the standard virtual overlay encapsulations (for example, VXLAN, NVGRE). The programmable header editor allows for supporting new emerging encapsulations, such as VXLAN-GPE, Geneve, and NSH.

The 98DX85xx provides an ideal platform for SDN and OpenFlow 2.0 applications, utilizing multiple TCAM lookups for generic match/action rules, large L2/L3 forwarding tables, and programmable header editor. The Marvell Forwarding Path Abstraction (FPA) software suite enables seamless integration with the leading OpenFlow agents and controllers.

Block Diagram



Marvell 98DX85xx Block Diagram

Key Features

Features	Benefits
Port Interface	• 24 ports of 25 GbE or 6 ports of 100 GbE • 48 ports of 1/2.5/5/10 GbE • 1 port of 10 GbE Port for CPU management
Bandwidth	• 1.08Tbps throughput with wire-speed processing of up to 600 million packets per second
Management I/O	• PCIe interface Gen 2.1 x1 • 1 Ethernet port of up to 10GbE for control traffic to the CPU
Highly Integrated	• Large forwarding tables • Large packet buff er memory • Shared TCAMs resources with Flexible TCAM sizes • High-speed SERDES
Forwarding Engines	• Layer-2 Wire-Speed Switching engine • Layer-3 Wire-Speed Routing engine • Virtual overlay networking – NVGRE, VXLAN-GPE, GENEVE, SPB, TRILL, GRE • Server Virtualization – IEEE 802.1Qbg EVB, 802.1BR Port Extender • NFV Service Function Chaining – Network Service Header (NSH) • Dynamic load balancing for optimizing elephant-flow distribution • Highly flexible TCAM Classifications engine • Hardware-based Operations, Administration, and Maintenance (OAM) engine
Quality of Service	• 1K QoS Profile to flexibly assign a packet traffic class, drop precedence, and packet CoS marking • 8 priority queues per physical port, with scheduling support for Strict Priority and Shaped Deficit Weighted Round-Robin (SDWRR) • Ingress/Egress Policers compliant with MEF 10.2 Single/Two Rate 3-Color Marking, and MEF 10.3 bandwidth sharing • Centralized traffic management with Remote Physical Ports
Precision Time Protocol (PTP)	• High accuracy one-step and two-step PTP compliant with IEEE 1588v1/v2

Target Applications

- Enterprise Campus LAN Access and Aggregation Switch
- Wi-Fi 802.11ac Wave2 Access Point Aggregation
- eDrive and Server connectivity
- Other interconnect applications requiring low-power 100 GbE, 40 GbE, 25 GbE, and 10 GbE embedded connectivity

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To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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