

# Marvell® Alaska® C MV-CHX9340P

Dual 800G, Quad 400G, Octal 200G, 16 port 100G Ethernet Transceiver with MACsec and Class C PTP

## Overview

The Marvell® Alaska® C MV-CHX9340P is the industry’s highest-performance and lowest-power single-chip 800 GbE PAM4 PHY transceiver capable of driving eight lanes of 106 Gbps PAM4 to support SR, DR, FR and LR optical links. The device performs IEEE 802.1AE MACsec encryption functionality for two ports of 800 GbE, four ports of 400 GbE, eight ports of 200 GbE or sixteen ports of 100 GbE. It also supports Class C PTP timestamping functionality as defined by IEEE 1588 v2 specifications. The device supports full duplex transmission at all supported speeds, over a variety of media including optics, passive direct attach (DAC) cables, active electric (AEC) cables and backplanes.

The device is targeted to next generation high density networking solutions based on 100G serial electrical signaling that requires MACsec, IPsec, PTP or Hitless Mux functionalities. The device also supports a variety of gearboxing modes to translate between 10G/25G NRZ, 50G PAM4 and 100G PAM4 modes for 800 GbE, 400 GbE, 200 GbE and 100 GbE, with the

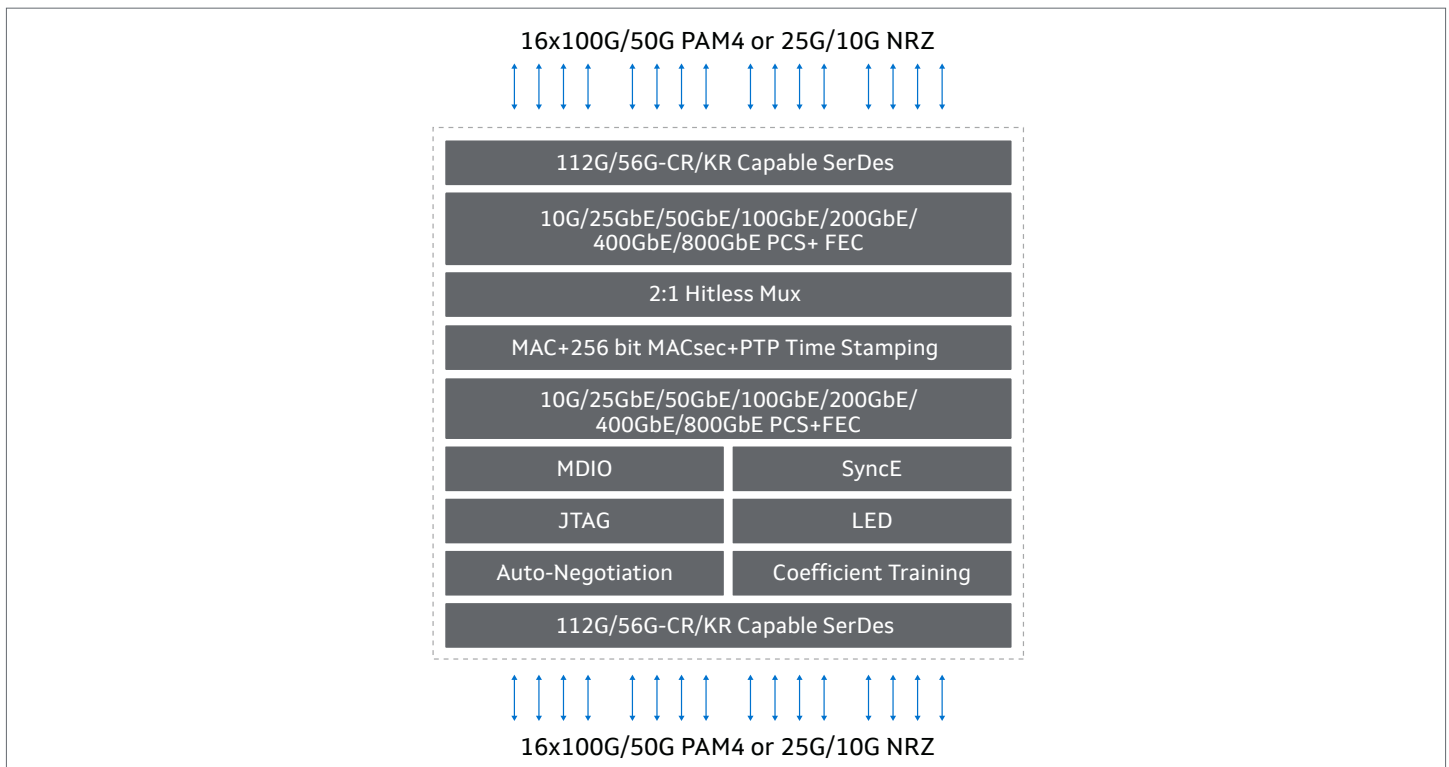
necessary FEC termination and regeneration capabilities for all FEC types including Clause-134 RS (544, 514), Clause-91 and Clause108 RS (528, 514) RS-FEC, and FC (2212, 2080) FEC.

The MV-CHX9340P has a fully symmetric architecture supports Auto-Negotiation and coefficient training capabilities on both host and line interfaces to provide complete system design flexibility, the AN/LT implementation is fully compliant to the IEEE 802.3 to support operation over KR backplanes and CR passive copper cables. The device is designed with a full 16x16 SerDes crossbar to support port multiplexing applications.

Internal registers can be accessed via an MDIO/MDC serial management interface which is compliant with the IEEE 802.3 specification (Clause 45).

The MV-CHX9340P is packaged in a 27 mm x 27 mm 841-pin FCBGA package with 0.9mm ball pitch.

## Block Diagram



## Key Features

Features	Benefits
Dual 800 GbE, Quad 400 GbE, Octal 200 GbE, 16-port 100 GbE MACSec with 256-bit key and Class C PTP	<ul style="list-style-type: none"><li>Enables encrypted links for all speeds from 1GbE up to 800GbE</li></ul>
Dual 400 GbE gearbox for translation from 4x100G PAM4 to 8x50G PAM4 switch PAM4	<ul style="list-style-type: none"><li>Enables support of 25G NRZ or 50G PAM4 I/O based optics from ASICs with 100G PAM4 I/Os. Also enables support of new 100G-optics with legacy switch ASICs</li></ul>
IEEE 1588v2 Class C PTP Timestamping that meets timing accuracy requirements for Class C PTP profile	<ul style="list-style-type: none"><li>Accurate extraction of timing information for timing critical applications</li></ul>
Recovered clock for SyncE applications with flexible selection of clock	<ul style="list-style-type: none"><li>Enables accurate transfer of clock over Ethernet networks</li></ul>
2:1 Mux on the host interface with hitless switching	<ul style="list-style-type: none"><li>For applications requiring Active/Standby redundancy with seamless switchover</li></ul>
Long Reach host and line interface SerDes	<ul style="list-style-type: none"><li>For driving DAC &amp; AEC cables and backplanes that exceeds the IEEE 802.3ck requirement for CR &amp; KR links</li></ul>
Fully symmetric architecture with FEC capability on host and line interfaces	<ul style="list-style-type: none"><li>Flexibility to support a wide range of applications and system design choices</li></ul>
Support for IEEE Auto Negotiation and Link Training protocol	<ul style="list-style-type: none"><li>Seamless interoperability with standards-compliant devices from other vendors</li></ul>
16x16 SerDes layer crossbar	<ul style="list-style-type: none"><li>Enables Port Multiplexing applications</li></ul>
Ethernet packet and PRBS generation capabilities and eye monitoring capabilities on all high-speed interfaces	<ul style="list-style-type: none"><li>Comprehensive test and debug capabilities</li></ul>

## Target Applications

**Hyperscale cloud data center networks:** High density switches and line cards application with gearbox or reverse gearbox capabilities.

**Enterprise and carrier core networks:** Build switches with MACsec & IPsec encryption and IEEE 1588v2 Class C PTP timestamping.



To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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